Mitigating of potential induced degradation (PID) using SiO$_2$ ARC layer

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Abstract: Potential induced degradation (PID) of photovoltaic (PV) cells in one of the most severe types of degradation, where the output power losses on solar cells level may even exceed 30%. In this article, we present the development of a suitable anti-reflection coating (ARC) structure of solar cells to mitigate the PID effect using SiO$_2$: ARC layer. Our PID testing experiments show that the proposed ARC layer can improve the durability and reliability of the solar cell, where the maximum drop in the efficiency was equal to 0.69% after 96h PID testing using an applied voltage of 1000 V and temperature set at 85 °C. In addition, we observed that the maximum losses in the current density are equal to 0.8 mA/cm$^2$, compared with 4.5 mA/cm$^2$ current density loss without using the SiO$_2$: ARC layer.

Keywords: Solar cells; PID mitigation; ARC; Electroluminescence imaging; Current density.

1. Introduction

Photovoltaic (PV) energy conversion based on crystalline silicon (c-Si) solar cells is one of the significant technological pillars for the tremendous success of the PV industry in the last decade. Confirmed terrestrial PV modules efficiencies of c-Si are above 24% and for multi-crystalline Si solar cells are as close as 20% [1].

The ways to improve the efficiency of solar cells is perpetually has been a challenging task since there is a strong interaction between the different recombination losses, including intrinsic and extrinsic recombination loss current density at maximum power point (MPP) as a function of the surface recombination at the rear side [2]. In addition, anti-reflection coating (ARC) structures of the solar cell also playing an essential role in shaping the maximum efficiency of the cell; an incorrect ARC structure can lead to a significant drop in the current density of more than 3.5 mA/cm$^2$ [3].

To keep the efficiency of solar cells at its highest levels, carefully, the reliability and stability must be checked. To facilitate this inspection, a potential induced degradation (PID) testing is exceedingly advised [4]. The PID test measures the leak current by applying a high voltage (normally 1000V and above, according to IEC 62804 standard) in a high temperature and humidity environment. After competing for the full duration of the test, 96h, the degradation of the PV module or on a small scale as a standalone solar cell can be measured by comparing the current-voltage (I-V) curve before the PID testing begins and after the PID test is fully complete [5].

In addition, the electroluminescent (EL) imaging can also be captured prior and after the PID test to visualize the actual collision on the surface structure after PID testing is done. EL imaging can also facilitate the overview of the cracks and defects of the cell, which is an immeasurable practice to provide [6].

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Current research expresses massive interest in mitigating PID problem of solar cells. This is principally due to three main reasons. First, the PID degrade the output power of the solar cells, and secondly, every solar cell affected by PID reduces the total string voltage [7]. Thirdly, it is complicated to make a fast detection of this problem when overall PV installations are up running [8], because degradation of PV output power is not only due to the impact of PID but also because of the existence of faulty bypass diodes [9], faulty PV modules [10-12], and hot-spots [13].

There are a number of ARC structures now available in the literature. However, a limited number of these structures have been under PID testing to check their reliability, stability, and degradation, hence, to ensure that the reported efficiencies are accurate. N-type solar cells structures, including BiSoN, MoSon, pPERT have been investigated by [14]. It was concluded that above mentioned ARC solar cell structures cannot mitigate the PID testing, and after 74h of PID testing, there is approximately 20% drop in the efficiency. Other experiments [15-16] have shown that p-type solar cells can degrade the efficiency in the range of 5% to 25%.

The investigation of bifacial PID in bifacial mono c-Si p-PERC solar cells was developed by [17]. It was evident that there is more considerable reduction in the efficiency of bifacial solar cells that have glass packing renders, which tends to be extremely sensitive to PID testing. Furthermore, the front side of bifacial solar cells tends to have more degradation compared with the rear junction. One of the solutions to mitigate PID effect on solar cells is to change the capsurlation film, instead of using ethylene vinyl acetate (EVA). Therefore, it is suggested by [18] to use Poly Olefin (PO) material with a low water vapour through rate. This solution, potentially, can reduce the power losses to around 3%. In addition, this new material was also proven to improve the reliability and stability of PV solar cells as demonstrated by [19]; they show that PO-made solar cells are resistant, to a certain degree, to the PID effect. Another research [20] suggests using thin silicon dioxide (SiO2) ARC layer in combination with p-type or n-type solar cells that can enhance the efficiency of the solar cell after applying PID test. There are some other recognized methods for mitigating PID effect on solar cells such as replacing the soda-lime glass with a quartz glass which guarantees the solar glass is free of the suspected PID ions [21]. Another appropriate method to mitigate the PID effect of solar cells is to attach a narrow, thin, flexible glass strips on the glass surface along the inner edges of the solar cell frame [22]. The drop of the output power after PID testing is equal to 8.8%, while it is equal to 15% prior using this mitigation technique.

An experimental evidence of PID effect on copper indium gallium selenide (CIGS) showed that CIGS PV cells suffer from PID testing [23]. The Reveled results show that there is almost 15% drop in the maximum output power after 120h of PID testing. In addition, it was also evident that the back and front contact almost have the same drop in the maximum power as well as the short circuit current after completing the PID testing cycle.

2. Gap of knowledge

Perhaps one of the most factors in today’s PV manufacturing systems and production is the reliability and stability of the used materials. We have seen a rapid growth of new ideas to mitigate PID effect of newly developed solar cell structures. However, there is still a lack of existing ARC structures that have been proven to be effective in mitigating PID. Therefore, in this article we present the development of a suitable ARC structure by layering SiO2 at the bottom of SiNx, which effectively reduces the PID affect. Results show that there is a limited drop in the maximum power of 0.01W; and the overall drop in the efficiency is limited at 0.69%, after 96h PID testing using an applied voltage of 1000 V and the temperature set at 85 °C.

3. Paper organization

The rest of the article is organized as follows: Section 4 presents the experiments to perform the PID testing on three different solar cells ARC structures. Section 5 presents the results of the PID testing on the PV cell SiO2-free layer, SiO2 layer placed at the top of SiNx, and the SiO2 layer placed at the bottom of SiNx. Lastly, Section 6 presents the overall conclusion of the results discussed in the article, followed by the acknowledgement and the reference list.
4. Experiment

In this study, a PID test was conducted by constructing three polycrystalline silicon solar cells with three types of ARC structures. The test was carried out using PIDcon PID-tester according to IEC 62804 standard, at 0h and after 96h. The working principles of the PIDcon test setup is shown in Figure 1.

The layer consists of a solar cell, polymer foil, and glass between the two metal electrodes. A positive voltage is applied at the upper electrode, while the bottom electrode is virtually grounded/heated. The shunt resistance ($R_{sh}$) as a function of time is also measured. The standard test condition followed, (i) voltage 1000V, (ii) temperature 85 °C, (iii) dry condition, no use of water, (iv) test duration 96 hours.

![Figure 1. A simple schematic of the working principles of the PIDcon test setup.](image)

The solar cells’ structure that has been tested in this study is shown in Figure 2. The first solar cell structure (Figure 2a) is made of a free SiO$_2$, while the second solar cell structure as in Figure 2b includes the SiO$_2$ thin film placed on the top of the silicon nitride (SiNx). The last solar cell is where the SiO$_2$ thin film is placed at the bottom of the SiNx. For ease of referencing, we called the first solar cell (cell #1), second (cell #2), and the third (cell #3).

To compare the PID of the three examined solar cells, first, we must identify the critical electrical parameters that have to be measured and compared. Here we complied with the IEC 62804 standard, hence, comparing the maximum power ($P_{max}$), Efficiency, and the short-circuit current density ($J_{sc}$). The efficiency was calculated using as the following ($FF$ is the fill factor, and $V_{oc}$ corresponds to the open-circuit voltage):

$$\text{Efficiency} = J_{sc} \times V_{oc} \times FF$$

![Figure 2. ARC structure of the three examined solar cells: (a) SiO$_2$-free layer (cell #1); (b) SiO$_2$ layer placed at the top of SiNx (cell #2); (c) SiO$_2$ layer placed at the bottom of SiNx (cell #3).](image)
4.1. SiO$_2$ layer preparation and properties

The SiO$_2$ thin film was prepared by liquid phased deposition. The deposition system contained temperature-controlled water to maintain uniformity in the deposition temperature amongst the surface and a Teflon vessel as a liquid solution. Initially, 25g of silica powder with 99.9% purity was mixed with 500 mL of hydrofluorosilicic acid; this mix was stirred for almost one-day long to ensure that the hydrofluorosilicic acid became saturated. The next step was to mix 32 mL of the saturated hydrofluorosilicic acid with 25 mL boric acid for the deposition of the SiO$_2$ film.

After the deposition process is completed, we have rinsed a tin-doped indium oxide glass in water; this process is required to make a purified nitrogen gas. Finally, the thin film was annealed at 425 °C in the air for 10 minutes. The chemical reaction between oxygen and silicon to generate SiO$_2$ is usually driven by a high-heat environment; however, even at room temperature, a shallow layer of native oxide, approximately 1nm thick can form in an air environment.

Illustrating the reasons for selecting the SiO$_2$ to mitigate the PID effect of solar cells are summarized as follows:

- It is straightforward to deposit on various materials and gown thermally on silicon wafers, which makes it manageable for manufacturing purposes.
- It can block the ion implementation of diffusion of many undesired contaminants, particularly when placed on the bottom of the SiN$_x$ layer.
- The interface between silicon and silicon dioxide has relatively few mechanical and electrical defects makes SiO$_2$ layer defect-free during the deposition process.
- It has high dielectric strength and a relatively wide bandgap, making it an excellent insulator.
- It has high-temperature stability of up to 1600 °C, making it a useful material for process and device integration [24].
- The SiO$_2$ layer causes the silicon-silicon dioxide interface to move into the wafer while the oxide grows, this would typically mean that while the oxide grows it consumes the silicon atoms at the surface of the wafer making it more reliable and structural layer.

4.2. Experiment setup (tools and equipment)

To perform the PID test on the solar cell samples, PIDcon PID-tester has been used. Main characteristics of this tester that no climate chamber is necessary during the PID test, no lamination of the solar cells is also required [25]. The leakage current, output power, and I-V curve also can be measured using this device. After the completion of the PID testing, the solar cells were subjected to EL imaging. This procedure has been accomplished using a high-resolution Keland EL tester. This device also allows the inspection of the current density of the solar cells. Therefore, by the end of each experiment, the I-V curve, EL and the current density images were analysed and compared.

The circuit diagram of the double diode model used for the analysis of the I-V curve measurements is shown in Figure 3. The junction recombination is modeled by adding a second diode $(D_2)$ in parallel with the first $(D_1)$ and setting the ideality factor typically to two.

![Figure 3. Circuit diagram of the double diode model including the series ($R_s$) and parallel ($R_{sh}$) resistances](image-url)
4.3. Performance of the examined solar cell samples before the PID testing

The electroluminescence (EL), current density and the I-V curves of the three solar cell samples before the PID test are shown in Figure 4. The critical parameters before the PID test began are summarized in Table 1, the efficiency of the cell #3 is equal to 19.24% (the lowest), and it is equal to 20.32% for the cell #2 (the highest). In addition, the value of the current density, open-circuit voltage and the fill factor are almost identical for the three solar cells samples.

Table 1. Summary of the critical parameters for the examined solar cells before the PID test.

<table>
<thead>
<tr>
<th>Sample</th>
<th>J_{sc} (mA/cm²)</th>
<th>V_{oc} (V)</th>
<th>FF (%)</th>
<th>P_{max} (W)</th>
<th>R_{sh} (Ω)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell #1</td>
<td>37.77</td>
<td>0.68</td>
<td>77.1</td>
<td>0.48</td>
<td>87.7</td>
<td>19.80</td>
</tr>
<tr>
<td>Cell #2</td>
<td>38.91</td>
<td>0.68</td>
<td>76.8</td>
<td>0.49</td>
<td>84.4</td>
<td>20.32</td>
</tr>
<tr>
<td>Cell #3</td>
<td>37.72</td>
<td>0.66</td>
<td>77.3</td>
<td>0.46</td>
<td>89.2</td>
<td>19.24</td>
</tr>
</tbody>
</table>

According to Figure 4, the EL image shows no cracks or significant defects in the examined solar cells before the PID test began. The current density images also show a uniform distribution of the current for all the samples, meaning no defects and leakage current is present. Seeing that the negative value of current density represents a reverse current following from the solar cell, zero current density represents no flow of current at a particular area of the cell, whereas the positive value of the current density shows a direct DC current generated by the cell.

Figure 4. EL, current density, and the I-V curve of the three examined solar cells before the PID test: (a) cell #1; (b) cell #2; (c) cell #3.
5. Results

5.1. SiO$_2$-free (cell #1)

After the completion of the PID test over 96 hours, the EL and the current density images were taken, as shown in Figure 5. It is evident that the solar cell had a considerable amount of degradation. As exhibited by the current density image, after the PID testing, there is a significant part of the solar cell that produces even negative current density, which typically results in a decrease in the efficiency of the cell.

![EL and the current density image of the first solar cell sample, SiO$_2$-free.](image)

Figure 5. EL and the current density image of the first solar cell sample, SiO$_2$-free.

Figure 6 shows the actual I-V curve of the solar cell before vs after the PID testing. The summary of the comparison between all relevant parameters is presented in Table 2. After the PID testing, all related parameters of the solar cell have significantly dropped. Remarkably, the efficiency of the solar cell became 13.96% (loss = 5.84%) compared with 19.80% before the PID testing (loss = 5.84%). Therefore, without the SiO$_2$ coating, the solar cell would potentially keep degrading over time.

The leakage current of this cell is generated continuously, so, PV modules made of SiO$_2$-free ARC structure would typically suffer from PID phenomenon, leading to poor stability and significant decay of the output power production, hence, continuous degradation over higher rates.

<table>
<thead>
<tr>
<th>Solar Cell #1</th>
<th>$J_{sc}$ (mA/cm$^2$)</th>
<th>$V_{oc}$ (V)</th>
<th>FF (%)</th>
<th>$P_{max}$ (W)</th>
<th>$R_{sh}$ (Ω)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before PID</td>
<td>37.77</td>
<td>0.68</td>
<td>77.1</td>
<td>0.48</td>
<td>87.7</td>
<td>19.80</td>
</tr>
<tr>
<td>After PID</td>
<td>33.2</td>
<td>0.66</td>
<td>63.7</td>
<td>0.37</td>
<td>9.12</td>
<td>13.96</td>
</tr>
</tbody>
</table>
5.2. SiO₂ thin film placed on the top of the SiNx (cell #2)

The I-V curve results of the PID testing for the second solar cell, which has a top-layer SiO₂ ARC structure is shown in Figure 7. This result reveals that placing the SiO₂ layer on the top of the SiNx does not have a significant impact on the stability of the solar cell, in fact, the experiment shows that the efficiency dropped by 7.03%; before PID 20.32% and after PID 13.29%. Other relevant parameters are presented in Table 3.

The EL and current density images of the cell are shown in Figure 8. According to the $J_{sc}$, the solar cell after completing the PID testing, it dropped from 38.91 mA/cm² to 31.90 mA/cm², approximately 18%. This result illustrates the negative impact of layering SiO₂ on the top of the SiNx.

In addition, the results of this experiment compared with cell #1 results are almost identical in terms of the drop in the shunt resistance from 84Ω to below 10Ω, and the drop in the FF from almost 75% to 63%. Thus, it is possible to assume that placing a layer of SiO₂ on the top of the SiNx leads to lowering $J_{sc}$ and $P_{max}$, consequently the cell efficiency.

In summary, both SiO₂-free and SiO₂ layer on the top of the SiNx solar cell samples had a significant leakage of the current after the PID testing complete. Therefore, this leads us to investigate another experiment which will be discussed in the next sub-section.

### Table 3. Before vs after PID testing of the first solar cell sample (cell #2).

<table>
<thead>
<tr>
<th>Solar Cell #1</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>$V_{oc}$ (V)</th>
<th>FF (%)</th>
<th>$P_{max}$ (W)</th>
<th>$R_{sh}$ (Ω)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before PID</td>
<td>38.91</td>
<td>0.68</td>
<td>76.8</td>
<td>0.49</td>
<td>84.4</td>
<td>20.32</td>
</tr>
<tr>
<td>After PID</td>
<td>31.90</td>
<td>0.66</td>
<td>63.1</td>
<td>0.35</td>
<td>7.51</td>
<td>13.29</td>
</tr>
</tbody>
</table>

Figure 6. I-V curve characteristics before and after the PID testing of the first solar cell sample, SiO₂-free.

Figure 7. I-V curve characteristics before and after the PID testing of the second solar cell sample, SiO₂-layer placed on the top of the SiNx.
5.3. SiO₂ thin film placed on the bottom of the SiNx (cell #3)

In this sub-section, the results of the PID testing of the third solar cell will be discussed. This solar cell has a SiO₂ layer placed on the bottom of the SiNx. Placing this layer on the bottom of the SiNx reasonably will achieve the following:

- Enhance the stability of the solar cell structure because there will be a limited leakage of the current as the top layer (SiNx), preventing mismatch conditions of the solar cell, particularly during the PID test [26].
- As there will be a limited leakage of the current, the expected drop in the efficiency will also be at a minimum level. In addition, it is expected to see a drop in the shunt resistance during the PID testing [27]. However, it will be a limited drop as the current density will remain at the highest.

Figure 9 shows the measured I-V curves before and after the PID testing for cell #3. There is a limited drop in the maximum power of 0.01W (approximately 2.2%); the efficiency also dropped by 0.69%; before PID 19.24% and after PID 18.55%. The shunt resistance dropped by 3.5Ω, representing a decrease of 3.92%. All interpretive parameters before and after the PID testing are presented in Table 4.

Table 4. Before vs after PID testing of the first solar cell sample (cell #3).

<table>
<thead>
<tr>
<th>Solar Cell #1</th>
<th>Jsc (mA/cm²)</th>
<th>Voc (V)</th>
<th>FF (%)</th>
<th>Pmax (W)</th>
<th>Rsh (Ω)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before PID</td>
<td>37.72</td>
<td>0.66</td>
<td>77.3</td>
<td>0.46</td>
<td>89.2</td>
<td>19.24</td>
</tr>
<tr>
<td>After PID</td>
<td>36.88</td>
<td>0.66</td>
<td>76.2</td>
<td>0.45</td>
<td>85.7</td>
<td>18.55</td>
</tr>
</tbody>
</table>

Figure 8. EL and the current density image of the second solar cell sample, SiO2 on the top of the SiNx.
The EL and current density images of the solar cell is shown in Figure 10. As can be noticed, there is a limited loss of approximately 2.2% in the current density after completing the PID test; before PID 37.72 mA/cm² and after PID 36.88 mA/cm², therefore, total loss 0.84 mA/cm².
Table 5 summarizes the percentage drop from before and after PID testing of each critical parameters analysed. Cell #3 shows lower drops for all parameters, reaffirming the effectiveness of using the SiO2 ARC layer for PID mitigation.

<table>
<thead>
<tr>
<th>Solar cell parameter</th>
<th>Cell #1</th>
<th>Cell #2</th>
<th>Cell #3</th>
</tr>
</thead>
<tbody>
<tr>
<td>J_sc</td>
<td>12.10%</td>
<td>18.00%</td>
<td>2.23%</td>
</tr>
<tr>
<td>V_oc</td>
<td>2.94%</td>
<td>2.94%</td>
<td>0%</td>
</tr>
<tr>
<td>FF</td>
<td>13.40%</td>
<td>13.70%</td>
<td>1.1%</td>
</tr>
<tr>
<td>P_max</td>
<td>22.92%</td>
<td>28.57%</td>
<td>2.17%</td>
</tr>
<tr>
<td>R_sh</td>
<td>89.60%</td>
<td>91.10%</td>
<td>3.92%</td>
</tr>
<tr>
<td>Efficiency</td>
<td>5.84%</td>
<td>7.03%</td>
<td>0.69%</td>
</tr>
</tbody>
</table>

In contrast with the above results, one of the decisive successes of the mitigating for PID testing when layering SiO2 on the bottom of the SiNx, the dark leakage current (J_sc) is extremely low due to the effective hydrogenation process, this would characteristically reduce the trapped charge density of the solar cell structures, therefore, improving the stability and reliability of the cell. In addition, PV modules consist of a series of those cells can also produce a resolute output power with a limited degradation over time.

6. Conclusions

In this article, we have discussed the potential of preventing PID by modifying the ARC structure in polycrystalline silicon solar cells. Three types of ARC structures were subjected to the PID test for a period of 96h under 1000V and 85 °C conditions, according to IEC 62804 standard. It was possible to conclude that the ARC structure containing SiO2-free or SiO2 layer on the top of the SiNx has a significant drop in the efficiency, always higher than 5%, after the PID test. A considerable value also decreases all other relevant parameters, including the shunt resistance (R_sh), short-circuit current density (J_sc) and the maximum output power (P_max).

We found that when the SiO2 layer is placed on the bottom of the SiNx, there is a limited leakage of the current of the solar cell after the completion of the PID test. Consequently, there was a limited drop in the maximum output power of 0.01W, which represents approximately to 2.2%, and the efficiency also dropped by 0.69%. Therefore, this ARC structure was confirmed to be an effective PID mitigation, preventing PV module degradation as well as increasing its reliability.

For future research, it would be interesting to perform the PID testing on a humidity environment since it is common to PV modules are subject to these conditions.

Author Contributions: M.D: formal analysis, Methodology, Software, Writing - original draft, Writing - review & editing. Y.H: methodology, Investigation, Writing - review & editing. N.S: Formal analysis, Supervision and Proofreading, Visualization, Writing - review & editing. R.V: Methodology, Writing - original draft, Writing - review & editing. All authors have read and agreed to the submitted version of the manuscript.

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